

In Place of FORM PTO-1449 (Modified)

Serial No.: ~~Not Yet Assigned~~

16/821,048

Applicants: Jente B. Kuang et al.

Filing Date: (herewith) 4/8/04

Group: ~~Not Yet Assigned~~

2819

Atty. Docket No.: AUS920040023US1

**LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANTS' INFORMATION DISCLOSURE
STATEMENT**

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
___ AAA						
___ ABA						
___ ACA						
___ ADA						
___ AEA						
___ AFA						
___ AGA						
___ AHA						
___ AIA						
___ AJA						
___ AKA						
___ ALA						
___ AMA						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
___ ANA						
___ AOA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner
Initial

APA

Rafik S. Guindi et al. "Design Techniques for Gate-Leakage Reduction in CMOS in Circuits," *IEEE*, 2003, 5 pages.

___ AQA

___ ARA

___ ASA

Examiner:

W. A. Kuang

Date Considered:

6/7/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

AUSTIN_1\245979\1
7047-P536US